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FIG 1A

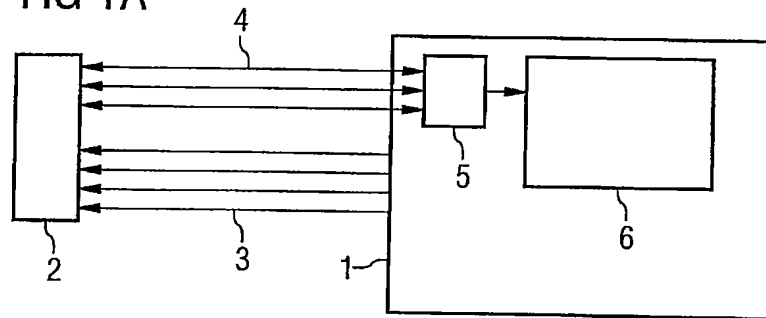


FIG 1B

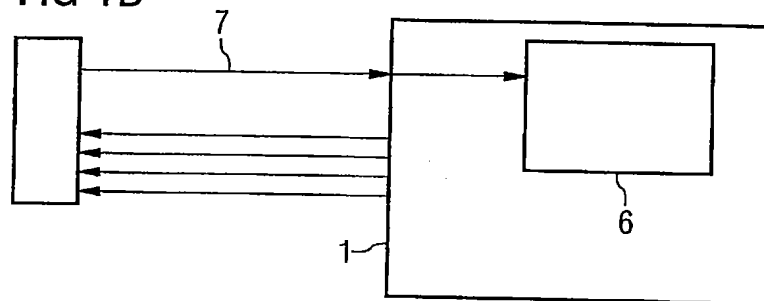
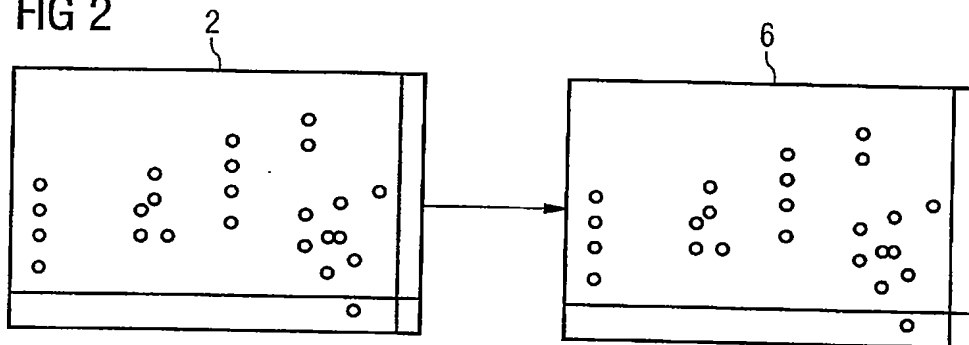


FIG 2



- 1-test device
- 2-memory module
- 3-address lines
- 4-data lines
- 5-comparator circuit
- 6-defect data memory
- 7-defect data line

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FIG 3A

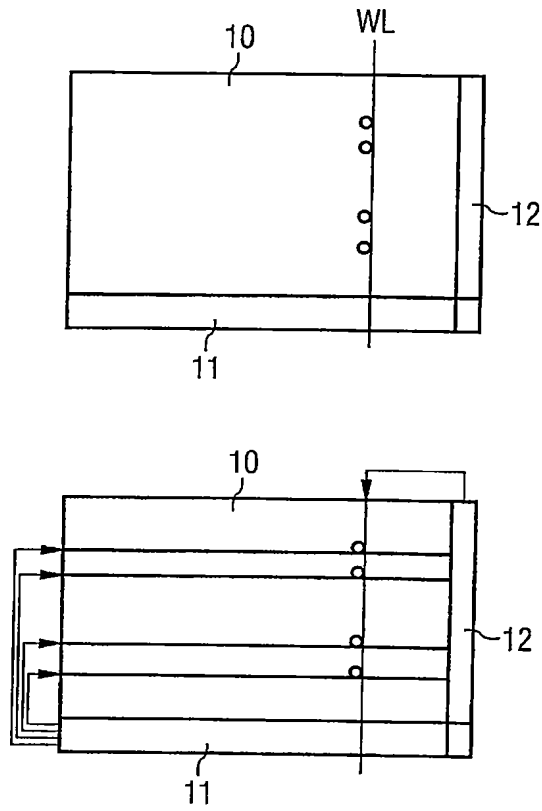
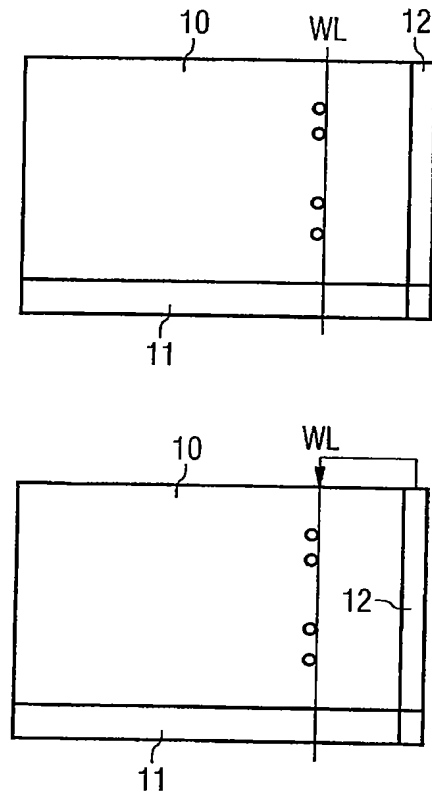


FIG 3B



10-memory cell array  
11- redundant bit line group  
12- redundant word line group

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FIG 4A

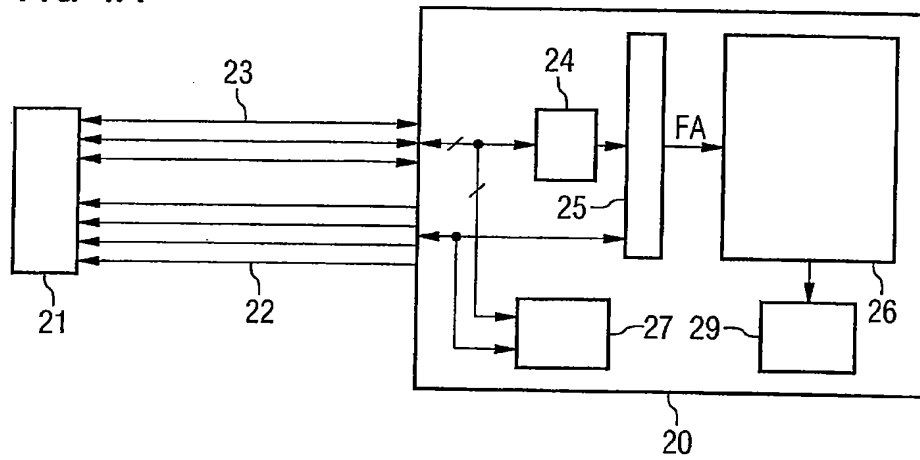
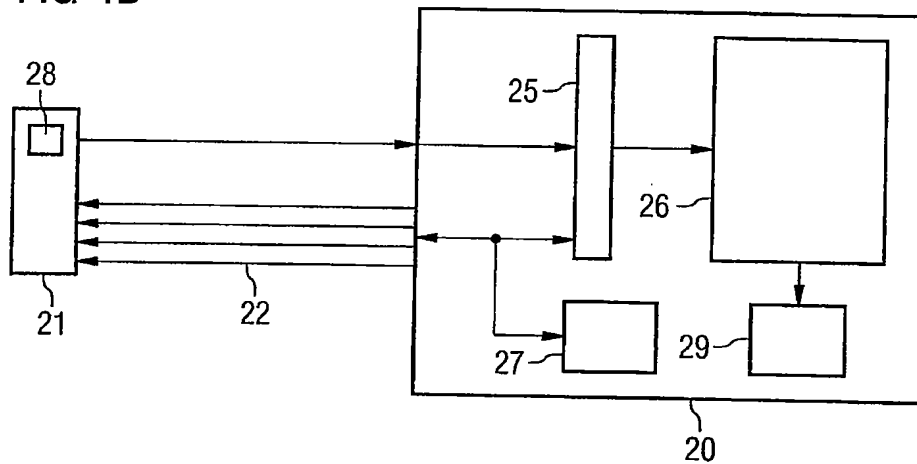


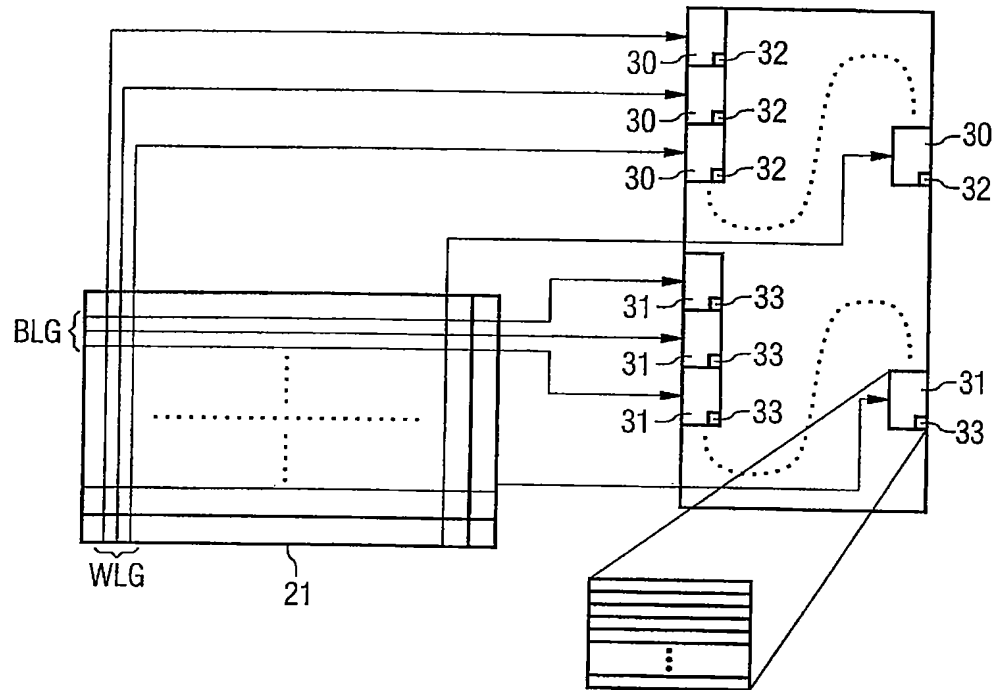
FIG 4B



- 21-memory module
- 22-address lines
- 23-data lines
- 24-comparator device
- 25-converter circuit
- 26-defect address memory
- 27-test control unit
- 28-second comparator circuit
- 29-evaluation unit

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FIG 5



21-memory module

30-first memory segment

31-second memory segment

32-first replacement register

33-second replacement register